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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
GRIER, LAURA A	

ART UNIT	PAPER NUMBER
2644	

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9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/730,200	KINDRED ET AL.	
	Examiner	Art Unit	
	Laura A Grier	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,36-45,50 and 51* is/are rejected.

7)☒ Claim(s) *29-35,46-49 and 53-59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5 and 6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-59 along with figure 1 in Paper No. 8 is acknowledged.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 9/2/03, and on 10/29/03 have been considered by the examiner.

Claim Objections

3. Claim 16 is objected to because of the following informalities: line 6, recites "the modulation". There is insufficient antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 37-42** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding **claim 37** (dependents 38-42), line 1 recites, "the filter", it unclear to the examiner as to which filter the claim language refers. In the independent claim 36, a filter of blocking low frequencies, and Hilbert filters are claimed. Thus, the claim language is indefinite.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claim 1-2, 5, 6, 7, 11 and 21-22** are rejected under 35 U.S.C. 102(b) as being anticipated by Flanagan et al., U. S. Patent No. 4071695.

Regarding **claim 1**, Flanagan et al. (herein, Flanagan) discloses a speech signal amplitude equalizer. Flanagan's disclosure comprises a speech signal source (301) that may contain an electroacoustic transducer (col. 2, lines 63-64), which reads on a microphone; a speaker is inherently provided as evident by the fact that the speech signal source is coupled to a communication device or network (260), wherein the speech input signal is processed to provide an audible output; and digital signal equalizer circuit which used modulation to produce an envelope of the speech signal via an envelope generator (305) coupled with components, such as peak detector (308) and threshold circuit (307) and a sum circuit (309; the adjustments a made via the output of the comparator (606), (figure 3 and 6, and col. 7, lines 50-68 and col. 8, 1-36, and 45-48), which reads on a processor to process the input sign at a gain, in which gain is evident by the fact that an envelope of the input signal is generated by the circuit, and reads an

adjuster for adjusting the gain, and reads on an inhibitor that inhibits distortion from modulation of the input signal.

Regarding **claim 2**, Flanagan discloses everything claimed as applied above (see claim 1). Flanagan further discloses the envelope generator (305) comprising two generators (328 and 331, respectively) for providing two representations that are orthogonal to each other in phase (col. 2, lines 15-20, col. 7, lines 61-68 – col. 8, lines 1-11).

Regarding **claim 5**, Flanagan discloses everything claimed as applied above (see claim 1). Flanagan further an estimator as evident by fact that the circuit comprises the envelope generator (305) comprising two generators (328 and 331, respectively) for providing two representations that are orthogonal to each other in phase (col. 2, lines 15-20, col. 7, lines 61-68 – col. 8, lines 1-11) and includes digital squarer circuit, digital summing circuit, and square root circuit (col. 8, lines 18-36).

Regarding **claim 6**, Flanagan discloses a speech signal amplitude equalizer. Flanagan's disclosure comprises a digital signal equalizer circuit which used modulation to produce an envelope of the speech signal via an envelope generator (305) coupled with components, such as peak detector (308) and threshold circuit (307) and a sum circuit (309); the adjustments a made via the output of the comparator (606), wherein an adjust is made if the envelope is greater than the theshold, and if the envelope is less than the threshold (figure 3, and 6, col. 7, lines 50-68, col. 8, 1-36, and 45-68, and col. 9, lines 1-30), which reads smoothing an envelope, and adjusting the gain based upon two conditions.

Regarding **claim 7**, Flanagan discloses everything claimed as applied above (see claim 2). Flanagan further discloses the envelope generator (305) comprising two generators (328 and

331, respectively) for providing two representations that are orthogonal to each other in phase (col. 2, lines 15-20, col. 7, lines 61-68 – col. 8, lines 1-11).

Regarding **claim 8**, Flanagan discloses everything claimed as applied above (see claim 2). Flanagan further discloses the envelope generator (305) comprising two generators (328 and 331, respectively) for providing two representations that are orthogonal to each other in phase, (col. 2, lines 15-20, col. 7, lines 61-68 – col. 8, lines 1-11), which provides inherent of creating the magnitude of the two representations to approximate the magnitude of the input signal, as evident by the fact that phase is characterized by magnitude.

Regarding claim 11, Flanagan et al. (herein, Flanagan) discloses a speech signal amplitude equalizer. Flanagan's disclosure includes a peak detector that receives a envelope signal from a signal envelope generator (105/205) and forms a smooth envelope of the envelope signal envelope generator (reference 208 and col. 5, lines 21-60), which reads on a detector; an adjustment is made the level of the signal via the comparators, operation amplifiers (507 and 509), where among two conditions are possible: one conditions is that envelope is greater than the threshold and the envelope being smaller or less than the envelope (col. 5, lines 51-68 and col. 6, lines 1-7), which reads on an adjuster, and the smooth envelope excluding modulation (col. 4, lines 24-68 and col. 5, lines 1-13).

Regarding claim 21, Flanagan discloses a speech signal amplitude equalizer. Flanagan's disclosure includes a peak detector that receives a envelope signal from a signal envelope generator (105/205) which includes a Hilbert transformation network (filter), (reference 208 and col. 5, lines 21-60), which reads on a detector; an adjustment is made the level of the signal via

the comparators - operation amplifiers (507 and 509), and a summing circuit (109/209), which reads on an adder, where among two conditions are possible: with one condition being than envelope greater than threshold, which represents the difference being greater than zero (col. 5, lines 51-68 and col. 6, lines 1-7), which reads on an adjuster.

Regarding claim 22, Flanagan discloses everything claimed as applied above (see claim 21). Flanagan further discloses that the frequency of the ranging between 0 to W Hz (col. 4, lines 28-29), which reads on a blocking low frequencies that are less than about 100 Hz.

8. **Claim 6** is rejected under 35 U.S.C. 102(b) as being anticipated by Yang, U. S. Patent No. 5706357.

Regarding claim 6, Yang discloses a signal input via a signal sound (10) coupled to a peak detector (110) of an over-modulator (100) for controlling peak level (envelope) of a signal input having a gain as evidence by the gain control amplifier (500) and gain control signal section (400), wherein the gain is adjusted if the peak level of the signal is greater than a predetermined level and when the peak level of the sound signal is lower the predetermined level (Col. 3, lines 39-64 and figures 2 and 4), which provides a method of smoothing and envelope, and adjusting the gain, therein.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 4, 9 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan.

Regarding **claim 4**, Flanagan discloses a peak detector in figure 3. However, figure 3 fails to include a Hilbert filter. However, in figure 2A of Flanagan, a Hilbert transformation network (filter) is used for smoothing the envelope signal. Thus it would have been obvious for one of ordinary skill in the art at time the invention was made to modify the invention by incorporating a Hilbert filter for the purpose of forming or to smooth an envelope of the imaginary part of an analytical signal as taught by figure 2A, as alternate way of smoothing the envelope of a gain signal.

Regarding **claim 9**, Flanagan discloses a peak detector in figure 3. However, figure 3 fails to include a Hilbert filter. However, in figure 2A of Flanagan, a Hilbert transformation network (filter) is used for smoothing the envelope signal. Thus it would have been obvious for one of ordinary skill in the art at time the invention was made to modify the invention by incorporating a Hilbert filter for the purpose of forming or to smooth an envelope of the imaginary part of an analytical signal as taught by figure 2A, as alternate way of smoothing the envelope of a gain signal.

Regarding **claim 10**, Flanagan discloses everything claimed as applied above (see claim 9). Flanagan further discloses the squarer circuits (229), a sum circuit (233) and a square root circuit (235), (col. 4, lines 36-68 and col. 5, lines 1-24).

11. **Claims 12 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan et al., U. S. Patent No. 4071695 in view of applicant's admitted prior art (herein, AAPA).

Regarding **claim 12**, Flanagan discloses everything claimed as applied above (see claim 11). Even though, Flanagan discloses that the speech signal source may contain an electroacoustic transducer (e.g. microphone) for providing the input signal, Flanagan fails to disclose a preamplifier having a gain to amplify the input signal.

Regarding the preamplifier, AAPA discloses on page 1, line 22-23, a preamplifier that is provided prior to processing section for the audio signal, wherein the preamplifier has a certain gain.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by implementing a preamplifier for the purpose of amplifying the signal output by the electroacoustic transducer of the speech signal source.

Regarding **claim 16**, Flanagan discloses a speech signal amplitude equalizer. Flanagan's disclosure includes a peak detector that receives an envelope signal from a signal envelope generator (105/205) and forms a smooth of the envelope signal envelope generator (reference 208 and col. 5, lines 21-60), which reads on a detector; an adjustment is made the level of the signal via the comparators, operation amplifiers (507 and 509), and sum circuit (109/209), where among two conditions are possible: one conditions is that envelope is greater than the threshold and the envelope being smaller or less than the envelope (col. 5, lines 51-68 and col. 6, lines 1-7), which reads on an adjuster, and the smooth envelope excluding modulation (col. 4, lines 24-

68 and col. 5, lines 1-13). Even though, Flanagan discloses that the speech signal source may contain an electroacoustic transducer (e.g. microphone) for providing the input signal, Flanagan fails to disclose a preamplifier having a gain to amplify the input signal.

Regarding the preamplifier, AAPA discloses on page 1, line 22-23, a preamplifier that is provided prior to processing section for the audio signal, wherein the preamplifier has a certain gain.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by implementing a preamplifier for the purpose of amplifying the signal output by the electroacoustic transducer of the speech signal source.

12. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan and AAPA as applied to claim 12 above, and further in view of Brennan et al., U. S. Patent No. 6240192.

Regarding **claim 13**, Flanagan and AAPA discloses everything claimed as applied above. Flanagan and AAPA fail to disclose an analog-to-digital converter.

Regarding an analog-to-digital converter (ADC), in a similar field of endeavor, Brennan et al. (herein, Brennan) discloses a digital hearing aid comprising an ADC (14) coupled to an output of a preamplifier (col. 3, lines 22-25).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan and AAPA by implementing an ADC for the purpose of converting the a preamplified acoustic signal to a digital representation as taught by Brennan.

13. **Claim 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan, AAPA and Brennan (herein, Flanagan combination) as applied to claim 13 above, and further in view of Williamson et al., U. S. Patent No. 5091952.

Regarding **claim 14**, Flanagan combination discloses everything claimed as applied above. Even though, Flanagan combination disclose a filter following the ADC, Flanagan fail to disclose the filter providing a filtered signal excluding direct-current components of the digitized input signal.

Regarding the filter, in a similar field of endeavor, Williamson et al. (herein, Williamson) discloses hearing aids with digital signal processing. Williamson discloses that after the digital conversion, the digital signal is applied to a filter, which filters out DC components (col. 5, lines 30-36), which reads on the filter.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan combination by incorporating a filter following the digital conversion for the purpose of filter out DC components and getting rid of DC offsets that may exist in the data of the signal as taught by Williamson.

Regarding claim 15, Flanagan combination and Williamson discloses everything claimed as applied above (see claim 14). Brennan , an ADC (14) coupled to an output of a preamplifier (col. 3, lines 22-25), and discloses a digital to analog convert (20) for converting the digital in an analog signal. However, Brennan fails to disclose a feedback of the analog signal to the audio input. However, Williamson ADC and DAC circuits as well and a feedback loop prior to audio output to input with the output signal of the microphone (col. 8, lines 5-47) for the purpose of

eliminating noise transients in the signal that may effect the gain level and acoustic sound to the signal.

14. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan and AAPA as applied to claim 16 above, and further in view of Williamson.

Regarding **claim 17**, Flanagan and AAPA discloses everything claimed as applied above. Even though, Flanagan discloses a filter for filtering the input signal, Flanagan fails to disclose the filter providing a filtered signal excluding direct current.

Regarding the filter, in a similar field of endeavor, Williamson et al. (herein, Williamson) discloses hearing aids. Williamson discloses the signal being applied to a filter, which filters out DC components (col. 5, lines 30-36), which reads on the filter.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan combination by incorporating a filter for the purpose of filter out DC components and getting rid of DC offsets that may exist in the data of the signal as taught by Williamson.

15. **Claims 18-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan, AAPA and Williamson (herein, Flanagan-Williamson) as applied to claim 17 above, and further in view of Orban, U. S. Patent No. 4495643.

Regarding **claim 18**, Flanagan-Williamson discloses everything claimed as applied above. Flanagan teaches the use of a Hilbert transform network (figure 2A and reference 225) coupled to the peak detector, which reads on the detector including a Hilbert filter; and the Hilbert transformation network does receive a filtered input signal. However, Flanagan-

Williamson fails to disclose the Hilbert transformation network producing two signals that are out of phase by 90 degrees with each other.

Regarding the Hilbert transformation network, in a similar field of endeavor, Orban discloses the use of Hilbert transforms and teaches the signal being divided into two signals with a 90 degree phase difference (col. 59-68 and col. 4, lines 16-24).

Thus it would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan-Williamson by providing the 90 degrees phase difference via the Hilbert transformation network (filter) for the purpose of forming an envelope of the imaginary part of an analytical signal as taught by Orban.

Regarding **claim 19**, Flanagan-Williamson and Orban discloses everything claimed as applied above (see claim 18). Flanagan discloses the squarer circuits (229), a sum circuit (233) and a square root circuit (235), (col. 4, lines 36-68 and col. 5, lines 1-24).

Regarding **claim 20**, Flanagan-Williamson and Orban discloses everything claimed as applied above (see claim 18). Flanagan discloses the squarer circuits (229), a sum circuit (223) and a square root circuit (235), (col. 4, lines 36-68 and col. 5, lines 1-24).

16. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan in view of Orban.

Regarding **claim 23**, Flanagan discloses everything claimed as applied above (see claim 22). Flanagan does disclose delay means (227 and col. 4, lines 67-68 and col. 1-2). However, Flanagan fails to disclose the delay means as being a digital delay element.

Regarding the digital delay element, in a similar field of endeavor, Orban discloses an audio limiting circuit that includes a delay means among the analog circuitry used for the invention, but further indicates in col. 9, lines 17-22 that digital circuitry may be used instead.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by implementing digital circuitry to incorporate a digital delay means or element for the purpose of providing enhancing processing speed of the circuits as taught by Orban.

17. **Claims 24-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan and Orban as applied to claim 23 above, and further in view of In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

Regarding **claim 24**, Flanagan and Orban discloses everything claimed as applied above (see claim 23). According the disclosure of Flanagan the Hilbert network (filter) does receives an input from the delay see col. 4, lines 67-68, and Orban teaches that delay may be placed before or after the Hilbert network (col. 4, lines 16-18). However, Flanagan and Orban fails to disclose second Hilbert transformation network (filter) to receive a delayed signal.

Regarding a second Hilbert filter, In re Harza states, "mere duplication of parts has no patentable significance unless a new and unexpected result is produced." Thus, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan and Orban by implementing a second Hilbert filter for acquiring the same the function of that of the 1st Hilbert network (filter).

Regarding **claim 25**, Flanagan and Orban and In re Harza disclose everything claimed as applied above (see claim 24). Flanagan discloses the squarer circuits (229), which reads on 1st and 2nd multipliers (col. 4, lines 36-68 and col. 5, lines 1-24, and figure 2).

Regarding **claim 26**, Flanagan and Orban and In re Harza disclose everything claimed as applied above (see claim 25). Flanagan discloses a sum circuit (233), which reads another adder (col. 4, lines 36-68 and col. 5, lines 1-24, and figure 2).

Regarding **claim 27**, Flanagan and Orban and in re Harza disclose everything claimed as applied above (see claim 26). Flanagan discloses a LPF (206), which constitutes as a limiter which is coupled to sum circuit 209.

18. **Claims 3, 28 and 36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan in view of Ludvigsen, U. S. Patent No. 6628795.

Regarding **claim 3**, Flanagan discloses everything claimed as applied above (see claim 1). However, Flanagan fails to disclose a multiple of time constants.

Regarding the time constants, in a similar field of endeavor, Ludvigsen discloses gain control comprising an adjusting means including attack time constant and release time constant (col. 5, lines 45-52).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by providing release and attack time constants to an inhibitor or adjusting means for the purpose of providing efficient automatic gain control by smoothing the envelope.

Regarding **claim 28**, Flanagan discloses speech signal amplitude equalizer. Flanagan's disclosure includes a peak detector that receives an envelope signal from a signal envelope generator (105/205), forms a smooth of the envelope signal output by envelope generator (reference 208 and col. 5, lines 21-60), which reads on a detector; and sum circuit (109/209), and comparators (507 and 509), and where among two conditions are possible (col. 5, lines 52-68 and col. 6, lines 1-20): one conditions is that when the envelope is greater than the threshold (E represents envelope and T represents threshold, wherein E > T), the comparator is effective to set (1) to flip-flop and when the envelope being smaller or less than the threshold (E represents envelope and T represents threshold, wherein E < T) , the comparator is effective to reset (0) flip-flop, (col. 5, lines 51-68 and col. 6, lines 1-7), wherein respect to the sum circuit if the difference result with a negative number, then logically the gain will be increased and likewise if the difference results with a positive number, then logically the gain will be decreased, reads on the adjuster to adjust gain, in which the gain adjust is evident by the fact that envelope signal is being generated from the input speech signal and input into a peak detector. However, Flanagan fails to disclose the adjuster receiving a release time constant and an attack time constant.

Regarding the adjuster receiving, a release time constant and an attack time constant, in a similar field of endeavor, Ludvigsen discloses gain control comprising an adjusting means including attack time constant and release time constant (col. 5, lines 45-52).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by providing release and attack time constants to the adjusting means for the purpose of providing efficient automatic gain control.

Regarding claim 36, Flanagan discloses speech signal amplitude equalizer. Flanagan's disclosure includes a filter (references 103/203 and col. 4, lines 25-35), which reads on blocking low frequencies (0 to W Hz) from the input signal; a signal envelope generator (105/205), which includes a Hilbert transformation network (filter), 225, forms a smooth of the envelope signal output by envelope generator, (col. 4, lines 24-68 and col. 5, lines 1-25), which reads on a detector; and sum circuit (109/209), and comparators (507 and 509), and where among two conditions are possible (col. 5, lines 52-68 and col. 6, lines 1-20): one conditions is that when the envelope is greater than the threshold (E represents envelope and T represents threshold, wherein $E > T$), the comparator is effective to set (1) to flip-flop and when the envelope being smaller or less than the threshold (E represents envelope and T represents threshold, wherein $E < T$) , the comparator is effective to reset (0) flip-flop, (col. 5, lines 51-68 and col. 6, lines 1-7), wherein respect to the sum circuit if the difference result with a negative number, then logically the gain will be increased and likewise if the difference results with a positive number, then logically the gain will be decreased, reads on the adjuster to adjust gain, in which the gain adjust is evident by the fact that envelope signal is being generated from the input speech signal and input into a peak detector. However, Flanagan fails to disclose the adjuster receiving a release time constant and an attack time constant.

Regarding the adjuster receiving, a release time constant and an attack time constant, in a similar field of endeavor, Ludvigsen discloses gain control comprising an adjusting means including attack time constant and release time constant (col. 5, lines 45-52).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by providing release and attack time constants to the adjusting means for the purpose of providing efficient automatic gain control.

19. **Claims 43-44** are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan and Ludvigsen and further in view of Klippel, U S. Patent No. 5528695.

Regarding claim 43, Flanagan discloses speech signal amplitude equalizer. Flanagan's disclosure includes a signal envelope generator (105/205), which includes a Hilbert transformation network (filter), 225, forms a smooth of the envelope signal output by envelope generator, (col. 4, lines 24-68 and col. 5, lines 1-25), which reads on a detector; and sum circuit (109/209), and comparators (507 and 509), and where among two conditions are possible (col. 5, lines 52-68 and col. 6, lines 1-20): one conditions is that when the envelope is greater than the threshold (E represents envelope and T represents threshold, wherein $E > T$), the comparator is effective to set (1) to flip-flop and when the envelope being smaller or less than the threshold (E represents envelope and T represents threshold, wherein $E < T$) , the comparator is effective to reset (0) flip-flop, (col. 5, lines 51-68 and col. 6, lines 1-7), wherein respect to the sum circuit if the difference result with a negative number, then logically the gain will be increased and likewise if the difference results with a positive number, then logically the gain will be decreased, reads on the adjuster to adjust gain, in which the gain adjust is evident by the fact that envelope signal is being generated from the input speech signal and input into a peak detector. However, Flanagan fails to disclose the adjuster receiving a release time constant and an attack time constant.

Regarding the adjuster receiving, a release time constant and an attack time constant, in a similar field of endeavor, Ludvigsen discloses gain control comprising an adjusting means including attack time constant and release time constant (col. 5, lines 45-52).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by providing release and attack time constants to the adjusting means for the purpose of providing efficient automatic gain control.

However, Klippel discloses the use of Hilbert transform(filter) that may be implemented using FIR filters or IIR filters (col. 4, lines 51-67), which reads on the IIR filters of envelope detection.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan and Ludvigsen by implementing IIF filters to the Hilbert Transformation for the purpose of enabling convenience of approximating a Hilbert Transform as taught by Klippel.

Regarding claim 44, Flanagan and Ludvigsen and Klippel disclose everything claimed as applied above (see claim 43). Klippel discloses indefinite impulse response filter as evident by the fact that is disclosed as an IIR-filter.

20. **Claim 45** is rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan, Ludvigsen, Klippel (herein, Flanagan et al.) and further in view of Akiho et al., U S. Patent No. 5524057.

Regarding claim 45, Flanagan et al. disclose everything claimed as applied above (see claim 44). However, Flanagan et al. fails to disclose the components of the IIR filter.

Regarding the components of the IIR filter, Akiho et al. discloses apparatus using IIR filters comprising a 1st and 2nd delay elements, and multipliers (figure 3 and col. 10, lines 15-35), which indicates 1st and 2nd delay element for delaying an input signal and the multipliers constitute as a scalar.

It would have been obvious to one of the ordinary skill in the art at the time the invention was mad to modify the invention of Flanagan et al. by providing the components of the IIR filter for the purpose of producing a modified or corrected signal as taught by Akiho et al.

21. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Flanagan et al., U. S. Patent No. 4071695 in view of Orban.

Regarding claim 50, Flanagan et al. (herein, Flanagan) discloses a speech signal amplitude equalizer. Flanagan disclosures includes a filter (references 103/203 and col. 4, lines 25-35), which reads on blocking low frequencies (0 to W Hz) from the input signal; a signal envelope generator (105/205) which develops a envelope that lacks modulation with use of Hilbert transform networks coupled with a comparators (507 and 509) for comparing the envelope and the threshold, and a summing circuit(109), (col. 4, lines 24-68, col. 5, lines 1-13, 45-68 and col. 6, lines 1-20), which reads forming an envelope that lacks modulation, and subtracting the envelope from the threshold to provide a difference control for controlling the gain. However, Flanagan et al. fails to disclose the input signal being a digitized.

Regarding the input signal being a digitized signal, in a similar field of endeavor, Orban discloses an audio limiting circuit that utilizes analog circuitry, but further indicates in col. 9, lines 17-22) that digital circuitry may be used instead.

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the invention of Flanagan by implementing digital circuitry components with means to digitize an input signal for the purpose of providing enhancing processing speed of the circuits as taught by Orban.

Regarding claim 51, Flanagan and Orban discloses everything claimed as applied above (see claim 50). Flanagan further discloses that the frequency of the ranging between 0 to W Hz (col. 4, lines 28-29), which reads on a blocking low frequencies that are less than about 100 Hz.

Regarding claim 52, Flanagan and Orban discloses everything claimed as applied above (see claim 50). Flanagan further indicates that difference is greater than zero (col. 52-68 and col. 6, lines 1-20).

Allowable Subject Matter

22. Claims 29-35, 46-49 and 53-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura A Grier whose telephone number is (703) 306-4819. The examiner can normally be reached on Monday - Friday, 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on (703) 305-4386.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

LAG
February 7, 2004